

INVENTORS DESIGNATION SHEET

TITLE: METHOD OF DECODING TURBO-ENCODED DATA AND RECEIVER FOR
DECODING TURBO-ENCODED DATA

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METHOD OF DECODING TURBO-ENCODED DATA
AND
RECEIVER FOR DECODING TURBO-ENCODED DATA

5 BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The invention relates to a method of decoding turbo-encoded data and a receiver for decoding turbo-encoded data both of which are suitable to a mobile communication system which operates in CDMA (Code Division Multiple Access).

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DESCRIPTION OF THE RELATED ART

There has been suggested a method of encoding data, called a turbo code, in which an error rate close to Shannon limit can be accomplished in encoding data, by C. Berrou et al.. This method is explained in detail, for instance, in Proceeding of International Conference of communication, pp. 1064-1070, May 1993.

The method of turbo-encoding data is characterized by the step of dividing a code having high complexity in decoding data, into a plurality of components each having low complexity in decoding data, to thereby successively enhance accuracy in decoding data by virtue of interaction among those components. Division of a code having high complexity in decoding data, into a plurality of components each having low complexity in decoding data is carried out by a maximum posterior probability (MAP) decoder which carries out soft-input and soft-output decoding.

25 BCJR (Bahl, Cocke, Jelinek and Raviv) algorithm is known as an algorithm for consistently accomplishing MAP decoding, but is accompanied with a problem of necessity of too much calculation. In order to reduce calculation, there have been suggested Max-Log MAP algorithm and SOVA (Soft-Output Viterbi Algorithm) both of which carry out approximate calculation. Herein,

Max-Log MAP algorithm which carries out approximation of calculation in BCJR algorithm in log area, and SOVA algorithm is a process to have soft-input and soft-output on the basis of Viterbi algorithm.

5 In CDMA mobile communication system, a control to power of a data transmitter is made in order to keep the power at minimum and increase system capacity as much as possible. In addition, since CDMA system can have a high gain in encoding data, by virtue of statistics multiple, enhancement in an ability of decoding data in a turbo decoder would bring a merit that the number of subscribers covered by the CDMA system can be increased.

10 However, the above-mentioned Max-Log MAP algorithm and SOVA algorithm are accompanied with a problem of degradation in characteristics thereof, though they can reduce calculation.

15 In order to solve the problem, there is known a method of carrying out calculation equivalent to BCJR algorithm, in log area, with reference to a table in which a correction term $fc(|\delta_1 - \delta_2|)$ is defined as a function of $(|\delta_1 - \delta_2|)$ in Max-Log MAP, based on Jacobian Logarithm.

$$\ln(e^{\delta_1} + e^{\delta_2}) = \max(\delta_1, \delta_2) + \ln(1 + e^{-|\delta_1 - \delta_2|}) = \max(\delta_1, \delta_2) + fc(|\delta_1 - \delta_2|) \quad \dots(1)$$

20 However, if the above-mentioned equation (1) were arranged into a table, it would be unavoidable for the table to become large in size.

For instance, hereinbelow is explained a process of updating alpha metric as an example. The alpha metric and above-mentioned beta metric and gamma metric correspond to α , β and γ , respectively, and are described in detail, for instance, in IEEE Transaction on Information Theory, pp. 284 287, 25 March 1974.

First, it is assumed that two alpha metrics selected on a trellis at that time are expressed as α_1 and α_2 , and values of the alpha metrics in a log area are expressed as $\alpha_{\log 1}$ and $\alpha_{\log 2}$. That is, α_1 and α_2 are expressed as follows.

$$\alpha_2 = \exp [\alpha_{\log 2}]$$

10 follows.

15

$$fc(|\delta_1 - \delta_2|) = \ln[1 + \exp\{\alpha_{\log 2} + \gamma_{\log 2} - \alpha_{\log 1} - \gamma_{\log 1}\}] \quad \dots(3)$$

Herein, the gamma metric is expressed as follows.

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signal having been extracted from the output signals transmitted from the second Viterbi decoder, and extracting data other than the control signal, from output signals transmitted from the first Viterbi decoder, at the first station.

Japanese Unexamined Patent Publication No. 6-261021, based on U.S.

- 5 Patent Application Serial No. 991841 filed on December 16, 1992, has suggested a device used in CDMA system in which encoded user signals are transmitted to each of a plurality of users, the user signals are produced by processing user signals with associated sequence of encoding coefficients, and a received signal includes a combination of the encoded user signals. The device is comprised of
- 10 means for receiving samples of the received signals received at a predetermined interval, and means for predicting users' symbols in response to the samples through the use of the extracted sequence of encoding coefficients. The sequence of encoding coefficients is defined as an interactive function of a sequence of encoding coefficients, associated with the users, and a sequence of encoding
- 15 coefficients, associated with other user.

Japanese Unexamined Patent Publication No. 2000-4196, based on U.S.

- Patent Application Serial No. 09/038721, has suggested a multiple access system of communication across a wireless interface, including a turbo encoder for turbo coding signal representations of packets of information, a transmitter for
- 20 transmitting a first signal representation of a first packet of information and a second signal including a re-transmission of part of the first signal and a new signal representation of a second packet of information, a receiver for receiving the signal representations, and a means for processing the signal representations by combining the transmitted signals with the re-transmitted signals to obtain an
- 25 output signal representation of the packet of information the transmitted and re transmitted signals being combined using rake processing.

The above-mentioned problems remain unsolved even in the above-mentioned Publications.

SUMMARY OF THE INVENTION

In view of the above-mentioned problems in the conventional turbo decoder used in CDMA mobile communication system, it is an object of the present invention to provide a method of decoding turbo-encoded, received data in CDMA system, which is capable of enhancing decoding performances with a minimum increase in a hard ware and a soft ware, exerting a minimum influence on a processing rate, and accomplishing a small-sized circuit with a light weight and small power consumption.

In one aspect, there is provided a method of decoding turbo-encoded, received data in CDMA (Code Division Multiple Access) system which carries out closed-loop control to electric power of a data transmitter, based on a signal to interference ratio, the method including the steps of (a) weighting reverse-diffused, received data, based on both the signal to interference ratio and data obtained when the signal to interference ratio is measured, (b) carrying out ACS operation or comparison/selection operation in a process of updating alpha metric, a process of updating beta metric, and a process for computing likelihood, to the thus weighted, received data, and (c) compensating for results of the ACS operation, based on a predetermined value associated with a difference generated when the ACS operation or the comparison/selection operation is carried out.

There is further provided a method of decoding turbo-encoded, received data in CDMA (Code Division Multiple Access) system which carries out closed-loop control to electric power of a data transmitter, based on a signal to interference ratio, the method including the steps of (a) weighting reverse-diffused, received data, based on both the signal to interference ratio and data obtained when the signal to interference ratio is measured, (b) carrying out ACS operation or comparison/selection operation in a process of updating alpha metric, a process of updating beta metric, and a process for computing likelihood, to the thus weighted, received data, and (c) compensating for results of the ACS operation in at least one of the process of updating alpha metric, the process of

updating beta metric, and the process for computing likelihood, based on a predetermined value associated with a difference generated when the ACS operation or the comparison/selection operation is carried out.

It is preferable that the step (a) is carried out in each of slot periods.

- 5 For instance, the step (a) may be designed to include a step of multiplying X with the reverse-diffused, received data, the X being defined as a value which is in proportion to a value obtained by dividing a root of a signal power per a slot by an interference power per a slot.

- 10 It is preferable that the comparison/selection operation is carried out by means of a subtracting circuit, and the results of the ACS operation are compensated for by means of a logic circuit which receives an output or an absolute value of an output transmitted from the subtracting circuit, and outputs a predetermined value in accordance with the output.

- 15 For instance, the step (a) may be carried out through a firmware defined by a processor for processing digital signals, and the step (c) may be carried out through a hardware including a logic gate.

- 20 In another aspect of the present invention, there is provided a receiver for decoding turbo-encoded, received data in CDMA (Code Division Multiple Access) system which carries out closed-loop control to electric power of a data transmitter, based on a signal to interference ratio, the receiver including (a) a power controller for weighting reverse-diffused, received data, based on both the signal to interference ratio and data obtained when the signal to interference ratio is measured, and (b) a turbo decoder which carries out ACS operation or comparison/selection operation in a process of updating alpha metric, a process of
25 updating beta metric, and a process for computing likelihood, to the thus weighted, received data, and compensates for results of the ACS operation, based on a predetermined value associated with a difference generated when the ACS operation or the comparison/selection operation is carried out.

There is further provided a receiver for decoding turbo-encoded,

received data in CDMA (Code Division Multiple Access) system which carries out closed-loop control to electric power of a data transmitter, based on a signal to interference ratio, the receiver including (a) a power controller for weighting reverse-diffused, received data, based on both the signal to interference ratio and
5 data obtained when the signal to interference ratio is measured, and (b) a turbo decoder which carries out ACS operation or comparison/selection operation in a process of updating alpha metric, a process of updating beta metric, and a process for computing likelihood, to the thus weighted, received data, and compensates for results of the ACS operation in at least one of the process of updating alpha metric,
10 the process of updating beta metric, and the process for computing likelihood, based on a predetermined value associated with a difference generated when the ACS operation or the comparison/selection operation is carried out.

It is preferable that the power controller carries out weighting reverse-diffused, received data in each of slot periods.

15 It is preferable that the power controller multiplies X with the reverse-diffused, received data, the X being defined as a value which is in proportion to a value obtained by dividing a root of a signal power per a slot by an interference power per a slot.

For instance, the turbo decoder may be comprised of (b1) a subtracting
20 circuit which carries out the comparison/selection operation, and (b2) a logic circuit which compensates for the results of the ACS operation, the logic circuit receiving an output or an absolute value of an output transmitted from the subtracting circuit, and outputting a predetermined value in accordance with the output

25 It is preferable that the power controller weights reverse-diffused, received data through a firmware defined by a processor for processing digital signals, and the turbo decoder compensates for the results of the ACS operation through a hardware including a logic gate.

In still another aspect of the present invention, there is provided a

combination of a turbo encoder for turbo-encoding data to be transmitted, and the above-mentioned receiver for decoding turbo-encoded, received data in CDMA (Code Division Multiple Access) system which carries out closed-loop control to electric power of a data transmitter, based on a signal to interference ratio, the turbo encoder including a plurality of component encoders arranged in parallel with one another.

For instance, the turbo encoder may be designed to include (a) first to N-th component encoders each of which receives data series to be encoded, wherein N is an integer equal to or greater than 2, (b) an interleaver connected to the component encoders in parallel to rearrange the data series in accordance with a predetermined rule, the interleaver receiving the data series and transmitting the data series to the second to N-th component encoders, and (c) a switch which switches parity series transmitted the component encoders.

There is further provided a combination of a turbo encoder for turbo-encoding data to be transmitted, and the above-mentioned receiver for decoding turbo-encoded, received data in CDMA (Code Division Multiple Access) system which carries out closed loop control to electric power of a data transmitter, based on a signal to interference ratio, the turbo encoder including a plurality of component encoders arranged in series.

For instance, the turbo encoder may be designed to include (a) an external encoder which receives data series to be encoded, (b) a puncturing circuit which punctures data series and parity series both transmitted from the external encoder, (c) an interleaver which rearranges bit arrangement in the data series and the parity series each in accordance with a predetermined rule, and (d) an internal encoder which receives the data series from the interleaver, and separates the data series and the parity series from each other.

In still another aspect of the present invention, there is provided a recording medium readable by a computer, storing a program therein for causing a computer to carry out the above-mentioned method of decoding turbo-encoded,

received data in CDMA (Code Division Multiple Access) system which carries out closed-loop control to electric power of a data transmitter, based on a signal to interference ratio.

There is further provided a recording medium readable by a computer, storing a program therein for causing a computer to act as the above-mentioned receiver for decoding turbo-encoded, received data in CDMA (Code Division Multiple Access) system which carries out closed-loop control to electric power of a data transmitter, based on a signal to interference ratio.

The advantages obtained by the aforementioned present invention will be described hereinbelow.

In accordance with the present invention, since data to be input into the turbo decoder includes data having been weighted in accordance with a signal to interference ratio, it would be possible to fabricate Jacobian table used for compensating for results of updating alpha metric, updating beta metric, and calculation of log likelihood, without data such as noise dispersion σ^2 and signal component E_s being included in the table.

Accordingly, it is possible to accomplish calculation equivalent to BCJR algorithm without a minimum influence being exerted on a processing rate, with just a minimum increase in hard ware. Hence, the present invention makes it possible in the CDMA mobile communication system to minimize power necessary for a transmitter to transmit signals, increase a capacity of the system to thereby increase the number of subscribers, and enhance a quality in receiving signals.

The above and other objects and advantageous features of the present invention will be made apparent from the following description made with reference to the accompanying drawings, in which like reference characters designate the same or similar parts throughout the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of an example of a receiver in CDMA mobile

communication system.

FIG. 2 is a block diagram of an example of a turbo encoder including a plurality of component encoders arranged in parallel with one another.

FIG. 3 is a block diagram of an example of a turbo decoder which
5 decodes data having been turbo-encoded by the turbo encoder illustrated in FIG. 2.

FIG. 4 is a block diagram of an example of the turbo decoder illustrated in FIG. 3 which turbo decoder is designed to be comprised of a single soft-input and soft-output decoder by resource sharing.

FIG. 5 is a block diagram illustrating an example of the soft-input and
10 soft-output decoder illustrated in FIGs. 3 and 4.

FIG. 6 is a block diagram of an example of the alpha metric producing circuit illustrated in FIG. 5.

FIG. 7 is a circuit diagram of an example of Jacobian table comprised of
15 logic circuits.

FIG. 8 is a graph showing a relation between input and output in the circuit illustrated in FIG. 7.

FIG. 9 is a block diagram of an example of the beta metric producing circuit illustrated in FIG. 5.

FIG. 10 is a block diagram of an example of the circuit for computing log
20 likelihood, illustrated in FIG. 5.

FIG. 11 is a block diagram of an example of a turbo encoder including a plurality of component encoders arranged in series with one another.

FIG. 12 is a block diagram of an example of a turbo decoder which
25 decodes data having been turbo-encoded by the turbo encoder illustrated in FIG. 11.

FIG. 13 illustrates examples of recording mediums in which a program for carrying out the method of decoding turbo-encoded data is to be stored.

phase in the complex number multiplier 103 are synthesized in the in-phase adder 104. That is, a plurality of the complex multipliers 103 and the in-phase adder 104 cooperate with each other to accomplish maximum ratio rake synthesis.

The weighting processor 106 measures signal power (S) and interference power (I) in each of passes through the use of pilot symbols, and computes a measured SIR value having been rake-synthesized, based on the signal power and interference power.

The interference power may be measured by averaging power associated with a plurality of slots, through a primary filter using an oblivion coefficient.

The weighting processor 106 computes a weighting coefficient defined in the following equation (6), for instance.

$$Q \times 2 \times (S_a)^{1/2} / (I_a) \quad (6)$$

In the equation (6), Q indicates a constant used for scaling a dynamic range of an output transmitted from the in-phase adder 104 which output is soft data for judgment, S_a indicates signal power per a slot, and I_a indicates interference power per a slot.

In the conventional method, rake-synthesized received data is transmitted to the turbo-decoder 110 without processing the rake-synthesized received data. In contrast, in accordance with the present embodiment, the multiplier 105 multiplies the rake-synthesized received data with a weighting coefficient used for controlling power of a data transmitter, and transmits the thus weighted received data to the turbo decoder 110.

The power controller 101 controls power of a data transmitter in each of slot periods so as to coincide the actually measured SIR with the target SIR. To this end, the subtracter 107 compares the actually measured SIR to the target SIR, and transmits the results of comparison to the comparator 108. The comparator 108 the comparison results received from the subtracter 107, into binary code, and thus produced binary code to the TPC command transmitter 109.

The TPC command transmitter 109 produces TPC commands by which power of a data transmitter is increased or decreased, in accordance with output signals transmitted from the comparator 108, inserts the thus produced TPC commands into a power control bit mapped in a frame of a descending link, and transmits the
5 TPC commands.

The above-mentioned closed-loop control to power of a data transmitter is carried out in each of slots. That is, a measured value of the received signal power and a measured value of the interference power which have been weighted are updated in each of slot periods.

10 A weighting coefficient added to the received signal in the weighting processor 106 is not to be limited to the coefficient defined in accordance with the above-mentioned equation (6). The weighting coefficient is dependent on gamma metric.

Hereinbelow is explained how a weighting coefficient is selected in a
15 process of updating alpha metric computed in the turbo decoder. A base of log is determined as a value associated with a predetermined Q-value.

First, it is assumed that two alpha metrics selected on a trellis at that time are expressed as α_1 and α_2 , and values of the alpha metrics in a log area in which a base is set equal to a predetermined constant A, are expressed as $\alpha_{\log 1}$
20 and $\alpha_{\log 2}$. That is, α_1 and α_2 are expressed as follows.

$$\alpha_1 = A \alpha^{\log 1}$$

$$\alpha_2 = A \alpha^{\log 2}$$

In addition, it is assumed that gamma metrics associated with the alpha metrics on a trellis are expressed as γ_1 and γ_2 , and values of the gamma
25 metrics in a log area are expressed as $\gamma_{\log 1}$ and $\gamma_{\log 2}$. It is assumed that an alpha metric having been updated is expressed as α_3 , and a value of the alpha metric α_3 in a log area is expressed as $\alpha_{\log 3}$.

As a result, the following equation (12) is obtained.

$$\alpha_{\log 3} = \alpha_{\log 1} + \left[\sum_i Y_i \cdot x_{1i} \right] + \log_A \left[1 + A^{\alpha_{\log 2} - \alpha_{\log 1} + \left[\sum_i Y_i \cdot x_{2i} \right] - \left[\sum_i Y_i \cdot x_{1i} \right]} \right] \quad \dots(12)$$

Accordingly, a term corresponding to the correction term $fc(|\delta_1 - \delta_2|)$ in the equation (12) is expressed as follows.

$$fc(|\delta_1 - \delta_2|) = \log_A \left[1 + A^{\alpha_{\log 2} - \alpha_{\log 1} + \left[\sum_i Y_i \cdot x_{2i} \right] - \left[\sum_i Y_i \cdot x_{1i} \right]} \right] \quad \dots(13)$$

Thus, the correction term $fc(|\delta_1 - \delta_2|)$ can be computed without including noise dispersion σ^2 and signal component Es therein both of which vary in accordance with phasing.

A difference in torclis corresponding to a sum of the alpha metric and the beta metric is represented as follows.

$$\alpha_{\log 2} - \alpha_{\log 1} + \left[\sum_i Y_i \cdot x_{2i} \right] - \left[\sum_i Y_i \cdot x_{1i} \right] \quad \dots(14)$$

By using the difference defined in accordance with the equation (14), it would be possible to readily fabricate Jacobian table in a small size to be used for the correction term $fc(|\delta_1 - \delta_2|)$.

The gamma metric to be processed in the turbo decoder 110 is expressed as follows.

$$\left[\sum_i Y_i \cdot x_i \right]$$

Since "x" is equal to 1 or 0, the above-mentioned gamma metric has a

value only in a pass associated with $x = 1$ on a torelis, and the gamma metric is equal to 0 in a pass associated with $x = 0$. Here, the weighting coefficient defined in accordance with the equation (6) is used as a weighting coefficient.

It is assumed that the gamma metric is expressed in accordance with the equation (15).

$$\gamma_{\log 1} = \log_A \left\{ \prod_i \frac{1}{\sqrt{2 \cdot \pi \cdot \sigma}} \exp \left[-\frac{\{y_i - \sqrt{E_s} \cdot (x_{1i})\}^2}{2 \cdot \sigma^2} \right] \right\} \quad \dots(15)$$

The equation (15) is substituted for the equation (8) to cancel common terms. As a result, the following equation (16) is obtained.

$$f_c(\delta_1 - \delta_2) = \log_A \left[1 + A \left\{ \alpha_{\log 2} - \alpha_{\log 1} + \log_A \exp \left[\sum_i \frac{\{y_i \cdot \sqrt{E_s} \cdot (x_{2i})\}}{\sigma^2} \right] - \log_A \exp \left[\sum_i \frac{\{y_i \cdot \sqrt{E_s} \cdot (x_{1i})\}}{\sigma^2} \right] \right\} \right] \quad \dots(16)$$

Herein, A is set equal to $\exp[1/Q]$, and the received data having been weighted is expressed Y_i which is determined as follows.

$$A = \exp [1/Q]$$

$$Y_i = y_i \cdot Q \cdot \frac{\sqrt{E_s}}{\sigma^2} \quad \dots(17)$$

Thus, there is obtained the following equation (18).

$$\alpha_{\log 3} - \alpha_{\log 1} + \left[\sum_i Y_i \cdot x_{1i} \right] + \log_A \left[1 + A^{\alpha_{\log 2} - \alpha_{\log 1} + \left[\sum_i Y_i \cdot x_{2i} \right] - \left[\sum_i Y_i \cdot x_{1i} \right]} \right] \quad \dots(18)$$

A difference on a torelis, associated with a sum of the alpha metric and the gamma metric is expressed as follows.

parity series include not only data transmitted from the turbo encoder illustrated in FIG. 2, but also soft-judged received data containing errors caused by passing through transmission mediums. In addition, the data series is multiplied with a weighting coefficient by the multiplier 105 illustrated in FIG. 1.

5 The parity series input into the separator 303 is separated into the first parity series and the second parity series. The first parity series is input into the first soft-input and soft-output decoder 302, and the second parity series is input into the second soft input and soft-output decoder 310.

As illustrated in FIG. 3, the data series and the pre-data log likelihood ratio (a priori 1) are added to each other in the first adder 301, and then, are input into the first soft-input and soft-output decoder 302. The pre-data log likelihood ratio (a priori 1) is designed to have an initial value of zero (0) so as not to have a preference. The first parity series separated from the parity series in the separator 303 is input also into the first soft-input and soft-output decoder 302.

10 The soft-input and soft-output decoder 302 outputs log likelihood ratios each associated with each of bits.

The second adder 306 subtracts both the pre-data log likelihood ratio (a priori 1) synchronized with an output transmitted from the first soft-input and soft-output decoder 302 by means of the first delay unit 304 and the data series synchronized with an output transmitted from the first soft-input and soft-output decoder 302 by means of the second delay unit 305, from the log likelihood ratio transmitted from the first soft-input and soft-output decoder 302. As a result, the second adder 306 transmits a first external data log likelihood consisting of the log likelihood from which both the data series and the pre-data log likelihood ratio (a priori 1) are removed.

15 The first external data log likelihood ratio is stirred in the first interleaver 307, and then, input into the third adder 309 together with the data series having been stirred by the second interleaver 308.

The second soft-input and soft-output decoder 310 receives an output

transmitted from the third adder 309 and the second parity series separated from the parity series in the separator 303. An output transmitted from the first interleaver 307 defines a pre-data log likelihood ratio (a priori 2) to be input into the second soft-input and soft-output decoder 310. The second soft-input and soft-output decoder 310 outputs log likelihood ratios associated with each of bits in the interleaved data series.

The fourth adder 313 subtracts both the pre-data log likelihood ratio (a priori 2) synchronized with an output transmitted from the second soft-input and soft-output decoder 310 by means of the third delay unit 311 and the interleaved data series synchronized with an output transmitted from the second soft-input and soft-output decoder 310 by means of the fourth delay unit 312, from the log likelihood ratio transmitted from the second soft-input and soft output decoder 310. As a result, the fourth adder 313 transmits a second external data log likelihood consisting of the log likelihood ratio from which both the interleaved data series and the pre-data log likelihood ratio (a priori 2) are removed.

The second external data log likelihood ratio is re-arranged back to its original bit arrangement by the first de interleaver 314, and then, fed back to the first soft-input and soft-output decoder 302 as the pre-data log likelihood ratio (a priori 1).

The data series, the first parity series and the second parity series are delayed by the fifth delay unit 315, and then, fed back in synchronization with the next updating step.

Hereinafter, the data series is decoded by repeatedly carrying out the above-mentioned steps through the use of fed back data series and parity series.

The log likelihood ratio transmitted from the second soft-input and soft-output decoder 310 is subject to hard judgment in the judge 316, and then, re-arranged back to its original bit arrangement in the second de-interleaver 317, and thereafter, output as decoded data.

FIG. 4 is a block diagram of an example of the turbo decoder illustrated

1 The external data log likelihood ratio is input into either the second
interleaver 410 or the first de-interleaver 411 in dependence on whether the soft-
input and soft-output decoder 401 operates at K-th times or L-th times. A
resultant output transmitted from either the second interleaver 410 or the first
5 de-interleaver 411 is fed back to the first delay unit 407 and the soft-input and
soft-output decoder 401 through the fourth switch 414 as the pre-data log
likelihood ratio.

Specifically, when the soft-input and soft-output decoder 401 operates
at K-th times, an output transmitted from the first de-interleaver 411 is fed back
10 as the pre-data log likelihood ratio, and when the soft-input and soft-output
decoder 401 operates at L-th times, an output transmitted from the second
interleaver 410 is fed back as the pre-data log likelihood ratio.

The first to fourth switches 404, 405, 413 and 414 is controlled in their
operation by control signals transmitted from a sequencer (not illustrated).

15 Hereinafter, the data series is decoded by repeatedly carrying out the
above-mentioned steps through the use of fed back data series and parity series.
The log likelihood ratio transmitted from the soft-input and soft-output decoder
401 is subject to hard judgment in the judge 412, and then, re-arranged back to its
original bit arrangement in the second de-interleaver 415, and thereafter, output
20 as decoded data.

Hereinbelow is explained the soft-input and soft-output decoder which
is a part of the turbo decoders illustrated in FIGs. 3 and 4. FIG. 5 is a block
diagram of an example of the soft-input and soft-output decoder illustrated in FIG.
3 and 4.

25 The soft-input and soft output decoder illustrated in FIG. 5 is
comprised of a gamma metric producing circuit 501 which produces gamma metric,
an alpha metric producing circuit 502 which produces alpha metric, a beta metric
producing circuit 503 which produces beta metric, and a log likelihood computing
circuit 504 which computes a log likelihood ratio, based on results of calculation

carried out by the alpha metric producing circuit 502 and the beta metric producing circuit 503.

Received data to be input into the soft-input and soft-output decoder is comprised of the data series resulting from multiplication of the rake-synthesized received data with the weighting coefficients, and correspond to the data series, the first parity series, and the second parity series all illustrated in FIGs. 3 and 4.

The turbo decoder illustrated in FIG. 3 is designed to have the two soft-input and soft-output decoders associated with the first and second parity series, and the turbo decoder illustrated in FIG. 4 is designed to have the single soft-input and soft-output decoder which alternately receives the first or second parity series. In contrast, in the soft-input and soft-output decoder illustrated in FIG. 5, the gamma metric producing circuit 501 is designed to include a memory (not illustrated) for storing the first and second parity series therein, and the first and second parity series is read alternately out of the memory.

In the turbo decoder illustrated in FIGs. 3 and 4, addition of the pre-data log likelihood ratio and the data series to each other is carried out outside the soft-input and soft-output decoder. In contrast, the addition is carried out in the gamma metric producing circuit 501 in the soft-input and soft-output decoder illustrated in FIG. 5.

In the turbo decoder illustrated in FIGs. 3 and 4, the pre-data log likelihood ratio and the data series are subtracted from the log likelihood ratio output from the soft-input and soft-output decoder, to thereby produce the external data likelihood ratio. The subtraction is carried out outside the soft-input and soft-output decoder. In contrast, the subtraction is carried out in the gamma metric producing circuit 501 in the soft-input and soft-output decoder illustrated in FIG. 5. Accordingly, gamma metric including the computed pre-data log likelihood ratio is input into both the alpha metric producing circuit 502 and the beta metric producing circuit 503.

An example of the gamma metric producing circuit 501 is disclosed, for

instance, in Japanese Unexamined Patent Publication No. 2001-24521. Hence, the gamma metric producing circuit will not be explained in detail. It should be noted that though the applicant refers to Japanese Unexamined Patent Publication No. 2001-24521, this does not mean that the applicant admits Japanese Unexamined Patent Publication No. 2001-24521 as prior art. Japanese Unexamined Patent Publication No. 2001-24521 is referred to herein only for the purpose of better understanding of the present invention.

Hereinbelow is explained the alpha metric producing circuit 502 with reference to FIG. 6.

FIG. 6 is a block diagram of an example of the alpha metric producing circuit 502 illustrated in FIG. 5.

The illustrated alpha metric producing circuit 502 is comprised of an add-compare select (ACS) circuit 601 which carries out predetermined operations such as addition, subtraction and comparison on which is greater, based on gamma metrics $\Gamma(0, 0)$, $\Gamma(1, 1)$, $\Gamma(1, 0)$ and $\Gamma(0, 1)$ transmitted from the gamma metric producing circuits 501, a memory 602 for storing therein alpha metrics produced by the ACS circuit 601, and an up-down counter 603 comprised of an address counter for controlling addresses used for storing alpha metrics.

ACS circuit 601 illustrated in FIG. 6 is designed to have a structure in order to carry out calculation for a metric including four states (S00, S01, S10, S11), completely in parallel with one another. ACS circuit 601 is applicable to calculation of an alpha metric including eight states, for instance.

In FIG. 6, signal points A and A', signal points B and B', signal points C and C', and signal points D and D' are connected to each other, respectively, and results of calculation of alpha metrics are fed back to a state register (S00, S01, S10, S11), and updated in the state register. The state register (S00, S01, S10, S11) in ACS circuit 601 and each of adders are connected through wires in accordance with a predetermined trellis chart.

ACS circuit 601 is comprised of the same four circuits which are

receives an input (a-b) equal to 7, the wired logic circuit outputs 3 as corrected data. For another instance, when the wired logic circuit receives an input (a-b) equal to 12, the wired logic circuit outputs 1 as corrected data.

An output transmitted from the selector SEL 11 and corrected data transmitted from the Jacobian table T11 are added to each other in an adder ADD 14. Calculation carried out in the adder ADD 14 corresponds to the calculation defined in accordance with the following equation (22).

$$\alpha_{\log 3} = \alpha_{\log 1} + \left[\sum_i Y_i \cdot x_{1i} \right] + \log_A \left[1 + A^{\sigma_{\log 2} - \sigma_{\log 1} + \left[\sum_i Y_i \cdot x_{2i} \right] - \left[\sum_i Y_i \cdot x_{1i} \right]} \right] \quad \dots(22)$$

The results of calculation carried out by the adder ADD 14 are stored in the memory 602, and further, fed back to the state register (S00).

The up-down counter 603 has a count width corresponding to a data bit length in a frame to be processed, and is incremented in each of data bits. A final bit in a frame to be processed defines a final address.

Data stored in the memory 602 is transmitted to the log likelihood computing circuit 504 at a predetermined timing.

Hereinbelow is explained the beta metric producing circuit 503 illustrated in FIG. 5, with reference to FIG. 9. FIG. 9 is a block diagram of an example of the beta metric producing circuit 503 illustrated in FIG. 5.

The illustrated beta metric producing circuit 503 is designed to include ACS circuit 901 which carries out calculation, based on the alpha and gamma metrics $\Gamma(0, 0)$, $\Gamma(1, 1)$, $\Gamma(1, 0)$ and $\Gamma(0, 1)$.

The alpha metric producing circuit 502 illustrated in FIG. 6 stores metrics in each of the states, in the memory 602. In contrast, the beta metric producing circuit 503 stores only a metric produced at a target time, in the state register (S00, S01, S10, S11) for updating. This is because a direction in which the alpha metric is updated is contrary to a direction in which the beta metric is updated. When a likelihood associated with a data bit at a target time, it would

be necessary to prepare both the alpha and beta metrics associated with the target time. To this end, at least one of the alpha and beta metrics has to include a memory.

In the alpha metric producing circuit 502 illustrated in FIG. 6 and the beta metric producing circuit 503 illustrated in FIG. 7, results of calculation of alpha metrics are stored in a memory, and a likelihood is computed in synchronization with updating beta metrics. In contrast, results of calculation of beta metrics may be stored in a memory, and a likelihood may be computed in synchronization with updating alpha metrics

Similarly to the alpha metric producing circuit 502 illustrated in FIG. 6, the beta metric producing circuit 503 illustrated in FIG. 9 is designed to have a structure in order to carry out calculation for a metric including four states (S00, S01, S10, S11), completely in parallel with one another. However, it should be noted that the beta metric producing circuit 503 is applicable to calculation of an beta metric including eight states, for instance.

In FIG. 9, signal points A and A', signal points B and B', signal points C and C', and signal points D and D' are connected to each other, respectively, and results of calculation of beta metrics are fed back to a state register (S00, S01, S10, S11), and updated in the state register. The state register (S00, S01, S10, S11) in ACS circuit 901 and each of adders are connected through wires in accordance with a predetermined trellis chart.

ACS circuit 901 is comprised of the same four circuits which are different from one another only in connection between the state register and the adder. Hereinbelow is explained an operation of the circuit located leftmost in FIG. 9. The circuit is designated as a unit block 902.

An output transmitted from the state register (S00), and a gamma metric $\Gamma(0, 0)$ are input into an adder ADD 21 in the unit block 902. An output transmitted from the state register (S01), and a gamma metric $\Gamma(1, 1)$ are input into an adder ADD 22 in the unit block 902.

Hereinbelow is explained the log likelihood computing circuit 504 illustrated in FIG. 5, with reference to FIG. 10.

FIG. 10 is a block diagram of an example of the log likelihood computing circuit 504 illustrated in FIG. 5.

5 As illustrated in FIG. 10, the log likelihood computing circuit 504 is designed to include a likelihood computing circuit 1001 which computes a likelihood, based on results of calculation carried out by both the alpha metric producing circuit and the beta metric producing circuit.

The result of adding the gamma and beta metrics, transmitted from the
10 beta metric producing circuit 503, and the alpha metric associated with the result, read out of the memory 602, are input into the likelihood computing circuit 1001. In general, alpha metrics are updated in an order of data bit arrangement in a received frame, and beta metrics are updated from a final bit. Hence, when a likelihood is computed in synchronization with calculation carried out in the beta
15 metric producing circuit, data is successively read out of the memory 602 firstly from a final address.

Though the present invention is applicable to a sliding window type likelihood computing circuit by replacing alpha metrics with new ones each time, there is used one shot type likelihood computing circuit herein for the purpose of
20 simplifying explanation.

Since the likelihood computing circuit 1001 illustrated in FIG. 10 carries out calculation in a signal direction, the calculation may be made in pipeline. For instance, a flip-flop (F/F) circuit may be incorporated into the likelihood computing circuit 1001. Hence, calculation for one data bit is carried
25 out per a clock.

The alpha metrics (α_{00} , α_{01} , α_{10} , α_{11}) read out of the memory 602, and a sum of the gamma and beta metrics transmitted from the beta metric producing circuit ($\beta_{00} + \Gamma(0, 0)$, $\beta_{00} + \Gamma(1, 1)$, $\beta_{01} + \Gamma(1, 1)$, $\beta_{01} + \Gamma(0, 0)$, $\beta_{10} + \Gamma(1, 0)$, $\beta_{10} + \Gamma(0, 1)$, $\beta_{11} + \Gamma(0, 1)$, $\beta_{11} + \Gamma(1, 0)$) are processed in

the likelihood computing circuit 1001 in accordance with a turelis chart, respectively.

In FIG. 10, hereinbelow is explained a turelis associated with data bit of "0".

5 A turelis associated with data bit of "0" corresponds to an output transmitted from an adder ADD 31, that is, a sum of $\alpha 00$ and $\beta 00 + \Gamma(0, 0)$ or an output transmitted from an adder ADD 32, that is, a sum of $\alpha 10$ and $\beta 01 + \Gamma(0, 0)$.

10 An adder (or subtractor) ADD 33 receives outputs transmitted from the adders ADD 31 and 32, and compares them to each other to detect which one is greater. Outputs transmitted from the adders ADD 31 and 32 are input into a selector SEL 31. The selector SEL 31 selects one of the outputs transmitted from the adders ADD 31 and 32 in accordance with results of comparison carried out by the adder ADD 33, and transmits the selected output.

15 The adder ADD 33 also outputs an absolute value of a difference between an output transmitted from the adder ADD 31 and an output transmitted from the adder ADD 32, to a Jacobian table T31.

The Jacobian table T31 is represented in accordance with the equation (25), and is comprised of wired logics such that the correction term $f_c(|\delta_1 - \delta_2|)$ is defined in accordance with the following equation (26).

$$\log_A [\alpha_1 \cdot \beta_1 \cdot \gamma_1 + \alpha_2 \cdot \beta_2 \cdot \gamma_2] = \log_A \left[(\alpha_1 \cdot \beta_1 \cdot \gamma_1) \cdot \left(1 + \frac{\alpha_2 \cdot \beta_2 \cdot \gamma_2}{\alpha_1 \cdot \beta_1 \cdot \gamma_1} \right) \right] \quad \dots(25)$$

$$\therefore L_{\log 1} = \alpha_{\log 1} + \beta_{\log 1} + \gamma_{\log 1} + \log_A \left[1 + A^{\{\alpha_{\log 2} + \beta_{\log 2} + \gamma_{\log 2} - \alpha_{\log 1} - \beta_{\log 1} - \gamma_{\log 1}\}} \right]$$

$$f_c(|\delta_1 - \delta_2|) = \log_A \left[1 + A^{\{\alpha_{\log 2} + \beta_{\log 2} + \gamma_{\log 2} - \alpha_{\log 1} - \beta_{\log 1} - \gamma_{\log 1}\}} \right] \quad \dots(26)$$

Similarly to the alpha metric producing circuit 502, the Jacobian table

is comprised of the wired logic circuits illustrated in FIG. 7, and has such I/O relation as illustrated in FIG. 8.

An output transmitted from the selector SEL 31 and corrected data transmitted from the Jacobian table T31 are added to each other in the adder
5 ADD 34. Calculation carried out in the adder ADD 34 corresponds to the calculation defined in the equation (25).

A toralis associated with data bit of "0" corresponds to an output transmitted from an adder ADD 35, that is, a sum of $\alpha 01$ and $\beta 11 + \Gamma(0, 1)$ or
10 $\Gamma(0, 1)$. an output transmitted from an adder ADD 36, that is, a sum of $\alpha 11$ and $\beta 10 +$

An adder (or subtractor) ADD 37 receives outputs transmitted from the adders ADD 35 and 36, and compares them to each other to detect which one is greater. Outputs transmitted from the adders ADD 35 and 36 are input into a selector SEL 32. The selector SEL 32 selects one of the outputs transmitted from
15 the adders ADD 35 and 36 in accordance with results of comparison carried out by the adder ADD 37, and transmits the selected output.

The adder ADD 37 also outputs an absolute value of a difference between an output transmitted from the adder ADD 35 and an output transmitted from the adder ADD 36, to a Jacobian table T32.

20 The Jacobian table T32 is represented in accordance with the equation (27), and is comprised of wired logics such that the correction term $fc(|\delta_3 - \delta_4|)$ is defined in accordance with the following equation (28).

$$\log_A [\alpha_3 \cdot \beta_3 \cdot \gamma_3 + \alpha_4 \cdot \beta_4 \cdot \gamma_4] = \log_A \left[(\alpha_3 \cdot \beta_3 \cdot \gamma_3) \cdot \left(1 + \frac{\alpha_4 \cdot \beta_4 \cdot \gamma_4}{\alpha_3 \cdot \beta_3 \cdot \gamma_3} \right) \right] \quad \dots (27)$$

$$\therefore L_{\log 4} = \alpha_{\log 3} + \beta_{\log 3} + \gamma_{\log 3} + \log_A \left[1 + A^{\{\alpha_{\log 4} + \beta_{\log 4} + \gamma_{\log 4} - \alpha_{\log 3} - \beta_{\log 3} - \gamma_{\log 3}\}} \right]$$

$$f_c(|\delta_3 - \delta_1|) = \log_A \left[1 + A^{\left\{ \alpha_{\log 4} + \beta_{\log 4} + \gamma_{\log 4} - \alpha_{\log 3} - \beta_{\log 3} - \gamma_{\log 3} \right\}} \right] \quad \dots(28)$$

Similarly to the alpha metric producing circuit 502, the Jacobian table T32 is comprised of the wired logic circuits illustrated in FIG. 7, and has such I/O relation as illustrated in FIG. 8.

5 An output transmitted from the selector SEL 32 and corrected data transmitted from the Jacobian table T32 are added to each other in the adder ADD 38. Calculation carried out in the adder ADD 38 corresponds to the calculation defined in the equation (27).

The above-mentioned torelis associated with data bit of "0" are
10 combined to each other. Specifically, an adder (or subtractor) ADD 39 receives outputs transmitted from the adders ADD 34 and 38, and compares them to each other to detect which one is greater. Outputs transmitted from the adders ADD 34 and 38 are input into a selector SEL 33. The selector SEL 33 selects one of the outputs transmitted from the adders ADD 34 and 38 in accordance with results of
15 comparison carried out by the adder ADD 39, and transmits the selected output.

The adder ADD 39 also outputs an absolute value of a difference between an output transmitted from the adder ADD 34 and an output transmitted from the adder ADD 38, to a Jacobian table T33.

The Jacobian table T33 is represented in accordance with the equation
20 (29), and is comprised of wired logics such that the correction term $f_c(|\delta_1 - \delta_2|)$ is defined in accordance with the following equation (30).

$$\log_A [I_1 + I_2] = \log_A \left[(L_1) \cdot \left(1 + \frac{L_1}{L_2} \right) \right] \quad \dots(29)$$

$$\therefore L_{\log p} = L_{\log 1} + \log_A \left[1 + A^{(L_{\log 1} - L_{\log 2})} \right]$$

$$f_c(\delta_1 - \delta_2) = \log_A \left[1 + A^{\{L_{\log 2} - L_{\log 1}\}} \right] \quad \dots(30)$$

Similarly to the alpha metric producing circuit 502, the Jacobian table T33 is comprised of the wired logic circuits illustrated in FIG. 7, and has such I/O relation as illustrated in FIG. 8.

5 An output transmitted from the selector SEL 33 and corrected data transmitted from the Jacobian table T33 are added to each other in the adder ADD 40. Calculation carried out in the adder ADD 40 corresponds to the calculation defined in the equation (29).

10 In the above-mentioned equations (29) and (30), it is assumed that δ_1 is equal to or greater than δ_2 ($\delta_1 \geq \delta_2$) in the terms selected by the selector SEL 33. That is, the equation (30) is established when $L_{\log 1}$ is equal to or greater than $L_{\log 2}$ ($L_{\log 1} \geq L_{\log 2}$). Hence, if the conditions for selection are reversed, exponential terms of A have to be changed accordingly.

Hereinbelow is explained a torelis associated with data bit of "1".

15 A torelis associated with data bit of "1" corresponds to an output transmitted from an adder ADD 41, that is, a sum of α_{10} and $\beta_{01} + \Gamma(1, 1)$ or an output transmitted from an adder ADD 42, that is, a sum of α_{00} and $\beta_{01} + \Gamma(1, 1)$.

20 An adder (or subtracter) ADD 43 receives outputs transmitted from the adders ADD 41 and 42, and compares them to each other to detect which one is greater. Outputs transmitted from the adders ADD 41 and 42 are input into a selector SEL 41. The selector SEL 41 selects one of the outputs transmitted from the adders ADD 41 and 42 in accordance with results of comparison carried out by the adder ADD 43, and transmits the selected output.

25 The adder ADD 43 also outputs an absolute value of a difference between an output transmitted from the adder ADD 41 and an output transmitted from the adder ADD 42, to a Jacobian table T41.

between an output transmitted from the adder ADD 45 and an output transmitted from the adder ADD 46, to a Jacobian table T42.

The Jacobian table T42 is represented in accordance with the equation (33), and is comprised of wired logics such that the correction term $fc(|\delta_3 - \delta_4|)$ is defined in accordance with the following equation (34).

$$\log_A[\alpha_3 \cdot \beta_3 \cdot \gamma_3 + \alpha_4 \cdot \beta_4 \cdot \gamma_4] = \log_A \left[(\alpha_3 \cdot \beta_3 \cdot \gamma_3) \cdot \left(1 + \frac{\alpha_4 \cdot \beta_4 \cdot \gamma_4}{\alpha_3 \cdot \beta_3 \cdot \gamma_3} \right) \right] \quad \dots(33)$$

$$\therefore L_{\log 2} = \alpha_{\log 3} + \beta_{\log 3} + \gamma_{\log 3} + \log_A \left[1 + A^{\{\alpha_{\log 4} + \beta_{\log 4} + \gamma_{\log 4} - \alpha_{\log 3} - \beta_{\log 3} - \gamma_{\log 3}\}} \right]$$

$$f_c(|\delta_3 - \delta_4|) = \log_A \left[1 + A^{\{\alpha_{\log 4} + \beta_{\log 4} + \gamma_{\log 4} - \alpha_{\log 3} - \beta_{\log 3} - \gamma_{\log 3}\}} \right] \quad \dots(34)$$

Similarly to the alpha metric producing circuit 502, the Jacobian table T42 is comprised of the wired logic circuits illustrated in FIG. 7, and has such I/O relation as illustrated in FIG. 8.

An output transmitted from the selector SEL 42 and corrected data transmitted from the Jacobian table T42 are added to each other in the adder ADD 48. Calculation carried out in the adder ADD 48 corresponds to the calculation defined in the equation (33).

The above-mentioned torelis associated with data bit of "1" are combined to each other. Specifically, an adder (or subtractor) ADD 49 receives outputs transmitted from the adders ADD 44 and 48, and compares them to each other to detect which one is greater. Outputs transmitted from the adders ADD 44 and 48 are input into a selector SEL 43. The selector SEL 43 selects one of the outputs transmitted from the adders ADD 44 and 48 in accordance with results of comparison carried out by the adder ADD 49, and transmits the selected output.

The adder ADD 49 also outputs an absolute value of a difference between an output transmitted from the adder ADD 44 and an output transmitted

from the adder ADD 48, to a Jacobian table T43.

The Jacobian table T43 is represented in accordance with the equation (35), and is comprised of wired logics such that the correction term $fc(|\delta_1 - \delta_2|)$ is defined in accordance with the following equation (36).

5

$$\log_A [L_1 + L_2] = \log_A \left[(L_1) \cdot \left(1 + \frac{L_2}{L_1} \right) \right] \quad \dots (35)$$

$$\therefore L_{\log M} = L_{\log 1} + \log_A \left[1 + A^{L_{\log 2} - L_{\log 1}} \right]$$

$$f_c(|\delta_1 - \delta_2|) = \log_A \left[1 + A^{\left\{ L_{\log 2} - L_{\log 1} \right\}} \right] \quad \dots (36)$$

Similarly to the alpha metric producing circuit 502, the Jacobian table T43 is comprised of the wired logic circuits illustrated in FIG. 7, and has such I/O relation as illustrated in FIG. 8.

10

An output transmitted from the selector SEL 43 and corrected data transmitted from the Jacobian table T43 are added to each other in the adder ADD 50. Calculation carried out in the adder ADD 50 corresponds to the calculation defined in the equation (35).

15

In the above-mentioned equations (35) and (36), it is assumed that δ_1 is equal to or greater than δ_2 ($\delta_1 \geq \delta_2$) in the terms selected by the selector SEL 33. That is, the equation (36) is established when $L_{\log 1}$ is equal to or greater than $L_{\log 2}$ ($L_{\log 1} \geq L_{\log 2}$). Hence, if the conditions for selection are reversed, exponential terms of A have to be changed accordingly.

20

An adder ADD 51 subtracts the output transmitted from the adder ADD 50, that is, the computation results $L_{\log M}$ associated with data bit of "1" from the output transmitted from the adder ADD 40, that is, the computation results $L_{\log P}$, to thereby compute the log likelihood ratio LLR output from the soft-input and soft-output decoder.

That is, the log likelihood ratio LLR is expressed as follows.

$$LLR = L_{\log P} - L_{\log M} \text{ ---- (37)}$$

The log likelihood ratio LLR is fed back also to the gamma metric producing circuit 502 illustrated in FIG. 5. As mentioned earlier, in the soft-input and soft-output decoder illustrated in FIG. 5, the pre-data likelihood ratio and the data series are subtracted from the log likelihood ratio LLR to thereby calculate the external data likelihood ratio in the gamma metric producing circuit 502. The thus calculated external data likelihood ratio is used as a next pre-data likelihood ratio.

Accordingly, by designing the alpha metric producing circuit, the beta metric producing circuit, and the log likelihood computing circuit to have a logic circuit defining the Jacobian table such as one illustrated in FIG. 7, it would be possible to carry out computation equivalent to BCJR algorithm, in a log area.

If performances are not degraded, at least one of the alpha metric producing circuit 502, the beta metric producing circuit 503, and the log likelihood computing circuit 504 may be designed not to include the Jacobian table, that is, not to compensate for received data, in order to reduce a size of the circuit.

Hereinbelow is explained a series arrangement type turbo encoder and a turbo decoder for decoding data which is turbo-encoded by the series arrangement type turbo encoder.

FIG. 11 is a block diagram of an example of a series arrangement type turbo encoder, and FIG. 12 is a block diagram of an example of a turbo decoder for decoding data encoded by the turbo encoder illustrated in FIG. 11.

The series arrangement type turbo encoder illustrated in FIG. 11 is comprised of an external encoder 1101 including at least one component encoder into which data series to be encoded is input, a puncturing circuit 1102 which punctures the data series and the parity series both transmitted from the external encoder 1101, an interleaver 1103 which re-arranges bit arrangement in the data series and the parity series each in accordance with a predetermined rule, and an

internal encoder 1104 including at least one component encoder and receiving the data series from the interleaver 1103.

The internal encoder 1104 and the external encoder 1101 both illustrated in FIG. 11 are designed to have the same structure. The data series and the parity series both transmitted from the external encoder 110 are input into the internal encoder 1104 through the puncturing circuit 1102 and the interleaver 1103.

A series arrangement type turbo encoder is usually designed to have a plurality of component encoders, similarly to the parallel arrangement type turbo encoder. The turbo encode illustrated in FIG. 11 is designed to have two component encoders.

Though the puncturing circuit 1102 and the interleaver 1103 play an important part in turbo encoding, their operation has nothing to do with the present invention, and hence, will not be explained in detail.

The puncturing circuit 1104 alternately removes bits in the parity series transmitted from the external encoder 1101. For instance, a sequence "11-10-10-11-10-" indicates significance of the data series and the parity series. Data "1" is output as it is, whereas data "0" is to be removed. That is, the second and fourth parity bits are removed in the above-mentioned sequence.

Because of alternate removal of parity bits by means of the puncturing circuit 1104, a data transmission rate in the external encoder 1101 is equal to $2/3$ per a unit period of time. However, since a data transmission rate in the internal encoder 1104 is equal to $1/2$, a total data transmission rate is equal to $1/3$ in a unit period of time.

The turbo decoder associated with the series arrangement type turbo encoder, illustrated in FIG. 12 is comprised of a first soft-input and soft-output decoder 1201 associated with the internal encoder 1104 illustrated in FIG. 11, a second soft-input and soft-output decoder 1206 associated with the external encoder 1101 illustrated in FIG. 11, a first de interleaver 1202 which re-arranges

bit arrangement in the data series transmitted from the first soft-input and soft-output decoder 1201, back to its original bit arrangement, a second de-interleaver 1204 which re-arranges bit arrangement in internal code data series or received data, back to its original bit arrangement, a first puncturing interpolator 1203
5 which zero-interpolates punctured bits, and outputs external code data series a-priori and external code parity series a-priori which are used for the second soft-input and soft-output decoder 1206 associated with the external encoder 1101, and a second puncturing interpolator 1205 which zero-interpolates punctured bits, and separates external code data series a-priori and external code parity series a-
10 priori from each other which are used for the second soft-input and soft-output decoder 1206 associated with the external encoder 1101.

Internal code data series and internal code parity series illustrated in FIG. 12 are comprised of data transmitted from the turbo encoder illustrated in FIG. 11 and soft-judged received data including errors generated by passing
15 through transmission mediums. The internal code data series and internal code parity series are data series with which a weighted coefficient is multiplied by the multiplier illustrated in FIG. 1.

The first soft-input and soft-output decoder 1201 receives the internal code data series, the internal code parity series, and the internal code data series a priori. Herein, the internal code data series a priori is designed to have an
20 initial value of zero (0) so as not to have preference.

The first soft-input and soft-output decoder 1201 outputs an external data log likelihood ratio consisting of a log likelihood ratio for each of bit in the internal code data series, from which the data series and the internal code data
25 series a priori are subtracted.

The external data log likelihood ratio output from the first soft-input and soft-output decoder 1201 is re-arranged by the first de-interleaver 1202 back to its original bit arrangement, zero-interpolated by the first puncturing interpolator 1203, and is separated into the external code data series a priori and

the external code data series a priori. The external code data series a priori and the external code data series a priori both output from the first puncturing interpolator 1203 are input into a second soft-input and soft-output decoder 1206.

5 The internal code data series is re-arranged by the second de-interleaver 1204 back to its original bit arrangement, zero-interpolated by the second puncturing interpolator 1205, and is separated into the external code data series and the external code data series. The external code data series and the external code data series both output from the second puncturing interpolator 1205 are input into the second soft-input and soft-output decoder 1206.

10 The external code data series a priori and the external code parity series a priori are used as a priori for the external code data series and the external code parity series, respectively.

15 The second soft-input and soft-output decoder 1206 outputs both an external code external data log likelihood ratio consisting of a log likelihood ratio for each of bits in the external code data series, from which the external code data series and the external code data series a priori are subtracted, and an external code external parity log likelihood ratio consisting of a log likelihood ratio for each of bits in the external code parity series, from which the external code parity series and the external code parity series a priori are subtracted.

20 The external code external log likelihood ratios correspond to an output transmitted from the external encoder illustrated in FIG. 11. The external code external log likelihood ratios transmitted from the second soft-input and soft-output decoder 1206 are input into the puncturing circuit 1207 and then the interleaver 1208, and output from the interleaver 1208 as a priori for the internal
25 code data series.

The thus produced internal code data series a priori is fed back to the first soft-input and soft-output decoder 1201, and is used as a priori for each of bits in the internal code data series.

Hereinafter, the same steps as mentioned above are repeatedly carried

out to thereby make hard judgment to a final log likelihood ratio, and resultingly, decoded data are output.

The series arrangement type soft-input and soft-output decoder has basically the same structure as that of the parallel arrangement type soft-input and soft-output decoder. Accordingly, the Jacobian tables in both the soft-input and soft-output decoders have the same structure. However, the second soft-input and soft-output decoder 1206 illustrated in FIG. 12 is structurally different from the parallel arrangement type turbo decoder as follows.

The first soft-input and soft-output decoder 1201 receives a priori associated with the data series. On the other hand, the second soft-input and soft-output decoder 1206 receives not only a priori associated with the data series, but also a priori associated with the parity series. Accordingly, the second soft-input and soft-output decoder 1206 is necessary to have such a structure that not only the data series a priori but also the parity series a priori are considered when a gamma metric is to be produced.

In addition, the log likelihood computing circuit is necessary to additionally include a circuit for outputting a log likelihood ratio of the parity series. Thus, it is necessary for the log likelihood computing circuit to include such output circuits one for the data series and the other for the parity series. However, by adding a small circuit to the single log likelihood computing circuit by resource sharing, it would be possible to compute two log likelihood ratios in a single log likelihood computing circuit. Specifically, in ACS circuit including the Jacobian table, the first stage subtraction circuit is commonly used for computing both a likelihood associated with data bit and a likelihood associated with parity hit, and the second and final stages subtraction circuits are fabricated separately for computing a likelihood associated with data bit, and for computing a likelihood associated with parity bit.

As mentioned above, the turbo decoder in accordance with the present invention makes it possible to accomplish computation equivalent to BCJR

algorithm merely by adding a small circuit thereto, without using algorithm accompanied with a problem of degradation in characteristics, such as Max-Log Map and SOVA.

Accordingly, in CDMA mobile communication system which can
5 accomplish a high gain in encoding data, it would be possible to minimize power for transmitting data, increase a capacity of the system, and enhance the number of subscribers and quality in receiving data.

In accordance with the invention, since rake-synthesized received data with which a weighting coefficient used for power control is multiplied is
10 transmitted to a hardware-structured turbo decoder, it is no longer necessary to have, as interfaces, noise dispersion and signal power which are necessary for accomplishing algorithm defined with Jacobian logarithm, and it is also no longer necessary for the turbo decoder to include a memory to store such interfaces therein.

Furthermore, it would be possible to carry out computation equivalent to BCJR algorithm which exerts less influence on an operation rate, merely by
15 further having a hardware at a minimum degree, without necessity of having a memory used for large-sized Jacobian table including noise dispersion and signal power as parameters.

The parallel arrangement type and series arrangement type turbo
20 decoders may be used without modification in an interface.

In addition, since a weighting step is carried out in each of slots, it would be possible to carry out the weighting step at an interval equal to an interval for updating transmission power control made based on SIR
25 measurement. This ensures minimum influence on a load to be exerted on DSP software, and accomplishment of algorithm defined by Jacobian logarithm following a phasing pitch.

The above-mentioned method of decoding turbo-encoded, received data in CDMA system may be accomplished as a program including various commands,

While the present invention has been described in connection with certain preferred embodiments, it is to be understood that the subject matter encompassed by way of the present invention is not to be limited to those specific embodiments. On the contrary, it is intended for the subject matter of the invention to include all alternatives, modifications and equivalents as can be included within the spirit and scope of the following claims.

The entire disclosure of Japanese Patent Application No. 2000 19747 filed on June 29, 2000 including specification, claims, drawings and summary is incorporated herein by reference in its entirety.